Title:

Reliable and Energy Efficient High Performance Computing (Finanziamento PNRR CN-HPC)

RESEARCH ACTIVITY

The research activity will be performed within the *Spoke "Future HPC" of the HPC, Big data e Quantum Computing National Research Center*. The research will be focused on the study and development of solutions for "Reliable and Energy Efficient High Performance Computing". In particular, HW and/or SW approaches for reliability evaluation, and HW techniques for enhanced reliability at low power will be developed for parallel open source (RiSC-V) processors.

ACTIVITY PLAN

The research will consist of the following phases:

1. Review of existing approaches for reliable and energy efficient high performance computing, with particular reference to parallel open source (RiSC-V) processors.
2. Analysis of the vulnerability of some critical components of RiSC-V processors to HW faults and aging conditions likely to affect their in-field operation
3. Evaluation of the effectiveness and costs (mainly in terms of power) of existing approaches identified at point 1 above in guaranteeing the tolerance and/or on-line monitoring of such faults and aging conditions.
4. Development of innovative approaches for the tolerance and/or on-line monitoring of faults and aging conditions at point 2 above, with respect to existing approaches evaluated at point 3 above.

While performing the research, the researcher will also consolidate and/or acquire her/his knowledge of CAD tools for electronic circuit and system fault/aging emulation and design (such as HSpice, Synopsys, etc).